Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (<u>Currently amended</u>) A method for displaying <u>and modifying timing data</u> generated by <u>an EDA tool used to simulate simulating</u> a circuit being designed by an EDA tool, the method comprising:

receiving the timing data from the EDA tool, the timing data including at least multiple periods of a plurality of clock signals,

selecting first and second <u>clock</u> signals <u>from the plurality of clock signals applied</u> to of nodes internal to the circuit based on input received from a user;

generating a first waveform for the first <u>selected clock</u> signal and a second waveform for the second selected clock signal using the timing data;[[,]]

generating a third waveform characterized as being a delayed replica of the first waveform and having transitions defining at least one launch edge;

generating a fourth waveform characterized as being a delayed replica of the second waveform and having transitions defining at least one latch edge;

selecting for display displaying a portion of each of the first, and second, third and fourth waveforms in a graphical user interface, wherein the displayed portion of each of the first and second third waveform displayed in the interface includes time points of interest to the user comprising the at least one launch edge and the displayed portion of the fourth waveform comprising the at least one latch edge;

displaying pointers to the time points of interest on the <u>displayed waveform</u> portions first and second waveforms;

receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface; and

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modifying the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edgeupdating timing parameters based on the edits to the time points of interest to simulate the circuit.

- 2. (Canceled)
- 3. (Canceled)
- 4. (Canceled)
- 5. (Currently amended) The method of claim [[3]] wherein:

the time duration of the displaying the portion of each of the first, and second.

third and fourth waveforms in a window of the interactive graphical user interface is a time

period selected to be a multiple of the least common multiple of periods comprises displaying a

launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal-at which the second storage element captures the data signal.

- 6. (Canceled)
- 7. (Canceled)
- 8. (Canceled)
- 9. (Currently amended) The method of claim 5-1 wherein: updating the timing parameters based on the edits to the time points of interest further comprises inverting the launch edge of the first clock signal, either in a design file or as an input to a static timing verification tool.
- 10. (Currently amended) The method of claim 5-1 wherein: updating the timing parameters based on the edits to the time points of interest further comprises inverting the latch edge of the second clock signal.

11. (Currently amended) A computer-readable medium encoded with a computer program, the computer program comprising a set of instructions for providing displaying and modifying timing data generated by simulating a circuit being designed using an EDA tool used to simulate a circuit being designed, wherein the set of instructions when executed by a computer causes the computer to:

receive the timing data from the EDA tool, the timing data including at least multiple periods of a plurality of clock signals,

enable selection of <u>first and second clock</u> signals <u>from the plurality of signals</u> applied to nodes internal to the circuit based on an input received from a user;

generate at least a first waveform for the first selected clock signal and a second waveform[[s]] for the second selected clock signal[[s]] using the timing data;[[,]]

generate a third waveform characterized as being a delayed replica of the first waveform and having transitions defining at least one launch edge;

generate a fourth waveform characterized as being a delayed replica of the second waveform and having transitions defining at least one latch edge;

select for display a portion of each of the at-least first, and second, third, and fourth waveforms in a interactive graphical user interface, wherein the displayed portion of each of the at least first and second waveforms displayed in the interactive graphical user interface includes time points of interest to the user the third waveform comprising the at least one launch edge and the displayed portion of the fourth waveform comprising the at least one latch edge;

display pointers to the time points of interest on the <u>displayed</u> waveform[[s]] portions;

generate new timing parameters based on receive edits to the time points of interest received from in response to a the user, wherein the user moves moving the pointers on the interactive graphical user interface to generate the edits; and

modify the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on edits to the time points of interest.

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generate updated waveforms for the signals using updated timing data, wherein the EDA tool generates the update timing data by compiling, simulating and performing verification analysis on the circuit design using the new timing parameters; and

display the updated waveforms in the interactive graphical user interface.

12. (Currently amended) The computer-readable medium according to claim 11 wherein[[:]]

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of each of the portions of the waveforms in synchronism.

- 13. (Canceled)
- 14. (Canceled)
- 15. (Canceled)
- 16. (Currently amended) The computer-readable medium according to claim 11[[5]] wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of a first pointer to a launch edge of the first third waveform that triggers a first latch to capture a data signal; and

display of a second pointer to a latch edge of the second-fourth waveform that triggers a second latch to capture the data signal.

17. (Currently amended) The computer-readable medium according to claim 16 wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of a third pointer to an edge of the third first waveform that corresponds to the launch edge source multi-cycle edge of the first waveform; and

display of a fourth pointer to an edge of the <u>fourth-second</u> waveform that corresponds to the <u>latch edge destination multi-cycle edge</u> of the second waveform.

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18. (Currently amended) The computer-readable medium according to claim 16 wherein the set of instructions when executed by the computer further causes the computer to generate[[s:]]

the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the second-first clock signal from the launch edge to the latch edge in response to the user moving the first or the second-third pointer on the interactive graphical user interface.

19. (Currently amended) The computer-readable medium according to claim 17 wherein the set of instructions when executed by the computer further causes the computer to generate[[s:]]

the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge in response to the user moving the third-second or the fourth pointer on the interactive graphical user interface.

- 20. (Previously presented) The computer-readable medium according to claim 11 wherein the circuit design is a design for a field programmable gate array.
- 21. (New) The computer readable medium according to claim 11 wherein the set of instructions when executed by the computer further causes the computer to generate updated waveforms for the signals using updated timing data, wherein the EDA tool generates the updated timing data by compiling, simulating and performing verification analysis on the circuit design using the new timing parameters and displays the updated waveforms in the interactive graphical user interface.